In the Claims:

Please amend claims 4, 7-13 and 21-26. Please cancel claims 1, 14, 15 and 27-30. The claims are as follows:

1. (Canceled)

2. (Previously Presented) A method of forming an isolation structure comprising, in the order recited:

(a) providing a semiconductor substrate;

(b) forming a buried N-doped region in said substrate;

(c) forming a vertical trench in said substrate, said trench extending into said N-doped region;

(d) removing said N-doped region to form a lateral trench communicating with and extending perpendicular to said vertical trench;

(e) partially filling said vertical and lateral trenches with a first insulating material;

(f) removing said first insulating material from said vertical trench;

(g) filling unfilled portions of said lateral trench and refilling said vertical trench with said first insulating material;

(h) removing said first insulating material from said vertical trench; and

(i) refilling said vertical trench with a second insulating material.

3. (Previously Presented) The method of claim 2, further including annealing said first insulating material in an inert atmosphere after steps (e) and (g) and annealing said first and second insulating material in an inert atmosphere after step (i).

4. (Currently Amended) The method of claim 2, wherein said first and second insulating materials are independently selected from the group consisting of ~~Silizane~~ spin-on-glass, Glass, TEOS and HDP oxide.

5. (Previously Presented) The method of claim 2, wherein said first insulating material is spun applied in steps (e) and (g).

6. (Canceled)

7. (Currently Amended) The method of claim [[6]] 2, wherein said first and second insulating materials are independently selected from the group consisting of TEOS and HDP oxide.

8. (Currently Amended) The method of claim [[1]] 2, further comprising:

before step (e), forming an insulating liner on all exposed surfaces of said vertical and lateral trenches.

9. (Currently Amended) The method of claim [[1]] 2, further comprising:

before step (b), forming an epitaxial silicon layer on said substrate.

10. (Currently Amended) The method of claim [[1]] 2, wherein said substrate is intrinsic or P-doped to a maximum concentration of 1E17 atm/cm^3 and said buried N-doped region are formed by ion implantation of an N-type dopant ion with a dose of 1E14 to 1E16 atm/cm^2.

11. (Currently Amended) The method of claim [[1]] 2, wherein said buried N-doped region is formed by ion implantation of arsenic, phosphorous or antimony or combinations thereof.

12. (Currently Amended) The method of claim [[1]] 2, wherein steps (c) and (d) are independently performed using one or more plasma etch processes.

13. (Currently Amended) The method claim [[1]] 2, further comprising:

forming an N-well or a P-well region in said substrate, said N-well or P-well partially bounded by said lateral trench; and

respectively forming the source and drain of an NFET or a PFET in said N-well or said P-well.

14. (Canceled)

15. (Previously Presented) A method of forming an isolation structure, comprising, in the order recited:

(a) forming a first patterned masking layer on a semiconductor substrate, whereby a portion of said substrate is exposed through an opening in said first masking layer;

(b) implanting ions into the exposed portion of said substrate thereby forming a buried N-doped region in said substrate;

(c) removing said first patterned masking layer and forming a second patterned masking layer on said substrate, an opening in said second patterned masking layer aligning over a less than whole portion of said buried N-doped region;

(d) etching a vertical trench in said substrate through said opening in said second patterned masking layer, said trench extending into said N-doped region;

(e) laterally etching said N-doped region to form a lateral trench communicating with and extending perpendicular to said vertical trench;

(f) partially filling said vertical and lateral trenches with a first insulating material;

(g) removing said first insulating material from said vertical trench;

(h) filling unfilled portions of said lateral trench and refilling said vertical trench with said first insulating material;

(i) removing said first insulating material from said vertical trench; and

(j) refilling said vertical trench with a second insulating material.

16. (Previously Presented) The method of claim 15, further including annealing said first insulating material in an inert atmosphere after steps (f) and (h) and annealing said first and said second insulating material in an inert atmosphere after (j).

17. (Original) The method of claim 15, wherein said first and second insulating material are independently selected from the group consisting of Spin-On-Glass, TEOS and HDP oxide.

18. (Previously Presented) The method of claim 15, wherein said first insulating material is spun applied in steps (f) and (h).

19. (Original) The method of claim 14 wherein step (f) comprises in the order recited:

(i) partially filling said vertical and lateral trenches with a first insulating material; and

(ii) completely filling said vertical and lateral trenches with a second insulating material.

20. (Original) The method of claim 19, wherein said first and second insulating materials are independently selected from the group consisting of TEOS and HDP oxide.

21. (Currently Amended) The method of claim [[14]] 15, further comprising:

before step (f), forming an insulating liner on all exposed surfaces of said vertical and lateral trenches.

22. (Currently Amended) The method of claim [[14]] 15, further comprising:

before step (b), forming an epitaxial silicon layer on said substrate.

23. (Currently Amended) The method of claim [[14]] 15, wherein said substrate is intrinsic or P-doped to a maximum concentration of 1E17 atm/cm^3 and said buried N-doped region are formed by ion implantation of an N-type dopant ion with a dose of 1E14 to 1E16 atm/cm^2.

24. (Currently Amended) The method of claim [[14]] 15, wherein said buried N-doped region is formed by ion implantation of arsenic or phosphorous.

25. (Currently Amended) The method of claim [[14]] 15, wherein steps (c) and (d) are independently performed using one or more plasma etch processes.

26. (Currently Amended) The method claim [[14]] 15, further comprising:

forming an N-well or a P-well region in said substrate, said N-well or P-well partially bounded by said lateral trench; and

respectively forming the source and drain of an NFET or a PFET in said N-well or said P-well.

27. – 30 (Canceled)